

*Sub E* *cont d*

37. (Amended) The apparatus of claim 4 wherein the duty cycle correction circuit is to receive the distributed clock signal and to generate a reference voltage signal, a voltage of the reference voltage signal to vary in response to a change in frequency of the distributed clock signal, the apparatus further comprising,

    a clock generation circuit to receive the reference voltage signal and to provide an output clock signal, the clock generation circuit to vary the delay of the output clock signal in response to a variation in voltage of the reference voltage signal.

#### REMARKS

Reconsideration of the present application is respectfully requested.

Claims 2-5, 7-11, 18-21 and 31-38 previously presented for examination remain in the application. Claims 2, 4-5, 7-9, 11, 18, 31, 33, and 35-37 have been amended. Claims 1, 6 and 28-30 have been cancelled without prejudice.

Claims 18-21 are allowed after addressing the § 112 rejection. Claims 4, 8 and 31-36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The Title stands objected to as considered to not be descriptive.

Applicants have changed the Title as indicated above in accordance with the Examiner's recommendation.

Claims 6-7, 18, 31, 33 and 35-36 stand objected to for minor informalities. Applicants have corrected the informalities as indicated in the above claim amendments. Applicants respectfully submit that the claims are in proper form.

Claims 37-38 stand rejected under 35 U.S.C. § 112, second paragraph as being considered to be indefinite. Applicants have amended claim 37 as indicated to more clearly and distinctly claim the subject matter that Applicants regard as the invention.

Claims 1-3, 5-7, 9-11, 28-30 and 37-38 stand rejected under 35 U.S.C. § 102(b) as being considered unpatentable over U.S. Patent No. 5,398,262 to Ahuja.

Claims 1, 6 and 28-30 have been cancelled rendering the rejection with respect to these claims moot.

Claims 4 and 8 have been amended to include all of the limitations of claim 1 and thus, should be found in condition for allowance.

Claims 2-3, 5 and 31-38 and claims 7, and 9-11 depend from and further limit claims 4 and 8 respectively and thus, should also be found in condition for allowance for at least the same reasons.

Based on the foregoing, applicants respectfully submit that the applicable rejections and objections have been overcome and claims 2-5, 7-11, 18-21, and 31-38 are in condition for allowance. If the examiner disagrees or believes that further discussion will expedite prosecution of this case, the examiner is invited to telephone applicants' representative at the number indicated below.

If there are any charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

Dated: Feb. 20, 2003

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I declare under penalty of perjury that the correspondence below is being deposited in the United States Postal Service with sufficient postage in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231

on 2.20.03 Date of Deposit  
Jerry Vicente Name of Person Mailing Correspondence  
Jerry Vicente 2.20.03 Signature Date

(Pencil)

**VERSION OF AMENDED CLAIMS WITH MARKINGS TO SHOW CHANGES**

2. (Amended) The apparatus of claim [1] 4 wherein the duty cycle correction circuit includes

a feedback path between an input and an output of the duty cycle correction circuit, the feedback path to control a delay of a circuit path in the duty cycle correction circuit to correct the duty cycle.

3. (Amended) The apparatus of claim 2 wherein the duty cycle of a corrected clock signal at an output of the duty cycle correction circuit is substantially equal to 50%.

4. (Amended) [The] An apparatus comprising: [of claim 1 further including]

a clock distribution network to distribute a clock signal on an integrated circuit chip;

a duty cycle correction circuit at a receiver in the clock distribution network, the duty cycle correction circuit to correct a duty cycle of a distributed clock signal received at the receiver; and

frequency multiplying circuitry coupled to the duty cycle correction circuit, the frequency multiplying circuitry to receive the distributed clock signal at an input and provide an output clock signal having a frequency that is a multiple of the distributed clock signal.

5. (Amended) The apparatus of claim [1] 4 further including a smart buffer circuit coupled to the duty cycle correction circuit, the smart buffer circuit to provide for proper operation of the duty cycle correction circuit over a range of loads to be coupled to the duty cycle correction circuit.

7. (Amended) The clock distribution network of claim [6] 8 wherein the clock distribution circuitry is further to distribute the global clock signal from the clock generation circuitry to a plurality of receiving points and wherein each of the plurality of receiving points [includes] is coupled to the duty cycle correction circuit.

8. (Amended) [The] A clock distribution network [of claim 7] comprising:

clock generation circuitry at a first location to generate a global clock signal;

clock distribution circuitry to distribute the global clock signal on an integrated circuit chip from the clock generation circuitry to a receiving point at a second, different location on the integrated circuit chip; and

a duty cycle correction circuit at the receiving point to correct the duty cycle of the distributed global clock signal received via the clock distribution circuitry.

wherein one of the receiving points further includes frequency multiplying circuitry coupled to the duty cycle correction circuit.

9. (Amended) The clock distribution network of claim [6] 8 wherein the duty cycle correction circuit includes a feedback path to control a delay of an output clock signal.

11. (Twice Amended) The clock distribution network of claim [6] 8 wherein the duty cycle correction circuit provides a corrected output clock signal having a substantially 50% duty cycle.

18. (Twice Amended) An integrated circuit chip comprising:  
a clock generation circuit to provide a first clock signal having a first duty cycle;  
a clock distribution network coupled to the clock generation circuit to distribute the first clock signal across the integrated circuit chip; and  
a plurality of duty cycle correction circuits at receiving points in the clock distribution network, the duty cycle correction circuits to correct a duty cycle of distributed [the] first clock signals at the receiving points.

31. (Amended) The apparatus of claim 2 further including:  
a sense amplifier in the feedback path, the sense amplifier having a threshold substantially equal to one half of the supply voltage (Vcc) to be coupled to the duty cycle correction circuit.

33. (New) The apparatus of claim [33] 32 wherein each of the reset path and the feedback path is coupled to control a variable delay element.

35. (Amended) The apparatus of claim 34 wherein the smart buffer includes

a first phase detector to detect a difference in delay between one of a rising or falling edge of the output signal and a corresponding edge of the reference signal, the first phase detector to provide a first reference control signal at [an] a first output, the first reference control signal to control a delay of a first delay element in the duty cycle correction circuit to adjust the drive strength of the driver for a first value of an input signal to the duty cycle correction circuit.

36. (Amended) The apparatus of claim 35 wherein the smart buffer circuit further includes

a second phase detector to detect a difference in delay between a remaining one of a rising or falling edge of the output signal and a corresponding edge of the reference signal, the second phase detector to provide a second reference control signal at [an] a second output, the second reference control signal to control a delay of a second delay element in the duty cycle correction circuit to adjust the drive strength of the output driver for a second value of the input signal to the duty cycle correction circuit.

37. (Amended) The apparatus of claim [1] 4 wherein the duty cycle correction circuit is to receive the distributed clock signal and to generate a reference voltage signal, a voltage of the reference voltage signal to vary in response to a change in frequency of the [input] distributed clock signal, the apparatus further comprising,

a clock generation circuit to receive the reference voltage signal and to provide an output clock signal, the clock generation circuit to vary the delay of the output clock signal in response to a variation in voltage of the reference voltage signal.